(d) a second transistor of the other of n-channel or p-channel type having a current path coupled between said input terminal and said control electrode of said first transistor and a control electrode; and

(e) circuitry coupled to said control electrode of said second transistor and responsive to one of said high signal and said low signal at said precharge node to control current flow in said current path of said second transistor.

Amend claim 3 as follows:

3. (Amended) The circuit of claim 1 wherein said circuitry coupled to said control electrode of said second transistor and responsive to the [status] state of said precharge node includes an inverter having an input coupled to said precharge node and an output and a feedback circuit coupled between said output and said control electrode of said second transistor.

Amend claim 10 as follows:

10. (Amended) The circuit of claim 2 wherein the control electrode of one of said pair of transistors is coupled to said control electrode of said [second] first transistor.

Amend claim 11 as follows:

11. (Amended) The circuit of claim 7 wherein the control electrode of one of said pair of transistors is coupled to said control electrode of said [second] first transistor.

Rewrite claims 12 to 14 in independent form as follows:

12. (Amended) A logic circuit which comprises:

a precharge node for retaining one of a high signal state and a relatively low signal;

an input terminal;

a first transistor of one of n-channel or p-channel type having a control electrode and a current path coupled between a source of power and said precharge terminal;

a second transistor of the other of n-channel or p-channel type having a current path coupled between said input terminal and said control electrode of said first transistor and a control electrode;

Q3 Contd

circuitry coupled to said control electrode of said second transistor and responsive to one of said high signal and said low signal at said precharge node to control current flow in said current path of said second transistor; and

a pair of transistors having serially connected current paths, said serially connected current paths being coupled between said precharge node and a reference source;

the control electrode of one of said pair of transistors being coupled to said control electrode of said first transistor;

[The circuit of claim 10] further including a fifth transistor of said one of n-channel or p-channel type having a current path in parallel with said second transistor and a control electrode coupled to said precharge node.

13. (Amended) A logic circuit which comprises:

a precharge node for retaining one of a high signal state and a relatively low signal;

an input terminal;

a first transistor of one of n-channel or p-channel type having a control electrode and a current path coupled between a source of power and said precharge terminal;

a second transistor of the other of n-channel or p-channel type having a current path coupled between said input terminal and said control electrode of said first transistor and a control electrode; and

circuitry coupled to said control electrode of said second transistor and responsive to one of said high signal and said low signal at said precharge node to control current flow in said current path of said second transistor;

Q3 cont'd

the control electrode of one of said pair of transistors being coupled to said control electrode of said first transistor;

said circuitry coupled to said control electrode of said second transistor and responsive to the status of said precharge node includes an inverter having an input coupled to said precharge node and an output and a feedback circuit coupled between said output and said control electrode of said second transistor;

said circuitry coupled to said control electrode of said second transistor and responsive to one of said high signal and said low signal at said precharge node includes an inverter having an input coupled to said precharge node and an output and a feedback circuit coupled between said output and said control electrode of said second transistor;

a third transistor of said one of n-channel or p-channel type coupled between a source of power and said control electrode of said second transistor and responsive to a said low signal at said output terminal to maintain said first transistor in an inactivated state;

[The circuit of claim 11] further including a fifth transistor of said one of n-channel or p-channel type having a current path in parallel with said second transistor and a control electrode coupled to said precharge node.

14. A logic circuit which comprises:

a precharge node for retaining one of a high signal state and a relatively low signal;

an input terminal;

a first transistor of one of n-channel or p-channel type having a control electrode and a current path coupled between a source of power and said precharge terminal;

a second transistor of the other of n-channel or p-channel type having a current path coupled between said input terminal and said control electrode of said first transistor and a control electrode;

Q3 contd

circuitry coupled to said control electrode of said second transistor and responsive to one of said high signal and said low signal at said precharge node to control current flow in said current path of said second transistor; and

a pair of transistors having serially connected current paths, said serially connected current paths being coupled between said precharge node and a reference source;

said circuitry coupled to said control electrode of said second transistor and responsive to the status of said precharge node including an inverter having an input coupled to said precharge node and an output and a feedback circuit coupled between said output and said control electrode of said second transistor;

[The circuit of claim 4] wherein the control electrode of one of said pair of transistors is coupled to a portion of a current path to said second transistor remote from said first transistor and further including a second inverter coupled to transmit current therethrough from said output of said inverter to said precharge node.

Add the following claims:

Q4 contd

21. A dynamic logic circuit, comprising:

a precharge transistor connected to a power source for precharging a node for indicating a first logic level upon receiving a precharge signal;

discharge means for discharging said node to indicate a second logic level; and

a switch for connecting said precharge signal to said precharge transistor, said switch connected to pass said precharge signal to said precharge transistor if said node has been prviously discharged to said second logic state.

22. A dynamic logic circuit as recited in claim 21, further comprising:

a keeper transistor connected between said power source and a gate of said precharge transistor for keeping said node at said first logic level prior to discharging with said discharging means.

23. A dynamic logic circuit as recited in claim 22 wherein a gate of said keeper transistor is connected to an output of said dynamic logic circuit.

24. A dynamic logic circuit as recited in claim 22, further comprising a half keeper latch comprising a transistor connected between said power source and said node and having a gate connected to an output of said dynamic logic circuit.

25. A dynamic logic circuit as recited in claim 23, further comprising a full keeper latch comprising:

a first transistor connected between said power source and said node and having a gate connected to an output of said dynamic logic circuit; and

a second transistor connected between said node and electrical ground, and having a gate connect to said output of said dynamic logic circuit.

26. A dynamic logic circuit as recited in claim 21 wherein said discharge means comprises a series of transistors for realizing a logical AND function.

27. a precharge circuit for a dynamic CMOS circuit, comprising:

a precharge node for holding a first voltage level indicating a first logic state;

a precharge transistor connected between said precharge node and a voltage source;

a keeper transistor connected between a gate of said precharge transistor and said voltage source for keeping said precharge node at said first voltage level indicating said first logic state prior to discharge; and

a switching transistor controlled by a feedback signal indicating a logic state of said precharge node; said switching transistor activating said precharge transistor during a stand-by cycle only if said precharge node has been previously discharged to a second voltage level indicating a second logic state.

28. A dynamic logic circuit as recited in claim 27 wherein a gate of said keeper transistor is connected to an output of said dynamic logic circuit.

29. A method of precharging a dynamic CMOS circuit, comprising the steps of:

precharging a node to a high voltage level indicating a first logic state during a stand-by mode;

discharging said node with connected logic circuitry if said logic circuitry is activated during an active mode;

precharging said node during a subsequent stand-by mode if said node was discharged during said discharging step; and

inhibiting the precharging of said node during said subsequent stand-by mode if said node remains precharged from a previous standy mode.